Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-5. (Cancelled).

C1

6. (Withdrawn) A method for manufacturing a semiconductor device made up of a pair of impurity regions each being used for a source and for a drain and being formed at intervals on a semiconductor substrate, a gate having a gate electrode formed on said semiconductor substrate used to control a drain current flowing between said impurity regions and side walls composed of insulating materials and formed on both sides of said gate electrode and a pair of electrode members formed on both sides of said gate on said semiconductor substrate and in a manner so as to be in contact with said side walls, comprising:

a step of forming a first impurity region below each of said electrode member by thermal diffusion of an impurity from each of said electrode members on said semiconductor substrate; and

a step of forming a second impurity region having a thickness being smaller than that of said first impurity region and extending from said first impurity region below said gate electrode by thermal diffusion of an impurity from said side walls on said semiconductor substrate and in a manner that said forming of said second impurity region proceeds in cooperation

with a reaction in said first impurity region.

7. (Withdrawn) A method for manufacturing a semiconductor device made up of a pair of impurity regions each being used for a source and for a drain and being formed at intervals on a semiconductor substrate, a gate having a gate electrode formed on said semiconductor substrate used to control a drain current flowing between said impurity regions and side walls composed of insulating materials and formed on both sides of said gate electrode and a pair of electrode members formed on both sides of said gate on said semiconductor substrate and in a manner so as to be in contact with said side walls, comprising:

a step of forming a first impurity region below each of said electrode member by thermal diffusion of an impurity from each of said electrode members on said semiconductor substrate; and

a step of forming a second impurity region having a thickness being smaller than that of said first impurity region and extending from said first impurity region below said gate electrode by thermal diffusion of an impurity from said side walls on said semiconductor substrate and in a manner that said forming of said second impurity region proceeds in cooperation with a reaction in said first impurity region, wherein said thermal diffusion employed to form each of said first and second impurity regions is simultaneously executed.

8. (Withdrawn) The method for manufacturing the semiconductor device according to Claim 6, wherein said thermal diffusion employed to form each of said first and second impurity regions is simultaneously executed by a RTA (Rapid Thermal Annealing) method.

9. (Withdrawn) The method for manufacturing the semiconductor

device according to Claim 6, wherein said forming process of said first impurity regions includes a step of stacking a silicon layer to be used for said pair of said electrode members on said semiconductor substrate, a step of causing said silicon to become a silicide, a step of implanting said impurity to be diffused into said silicide and a step of performing heating processing on said semiconductor substrate to thermally diffuse said impurity to said semiconductor substrate from said pair of said electrode members obtained by performing patterning operations on said silicon layer with said impurity implanted.

C1 Cont.

10. (Withdrawn) The method for manufacturing the semiconductor device according to Claim 6, wherein said forming process of said second impurity regions includes a step of stacking an insulating material to be used for said pair of said side walls on said semiconductor substrate, a step of implanting said impurity to be diffused into a stacked layer composed of said insulating material and a step of performing heating processing on said semiconductor substrate to thermally diffuse said impurity to said semiconductor substrate from said pair of said side walls obtained by performing patterning operations on said stacked layer with said impurity implanted.

11. (Withdrawn) The method for manufacturing the semiconductor device according to Claim 9, wherein said silicon layer to be used for said electrode members is formed by a CVD (Chemical Vapor Deposition) method.

12. (Withdrawn) The method for manufacturing the semiconductor device according to Claim 9, wherein said process of causing said silicon layer to become said silicide includes a step of stacking a metal material on said silicon layer by a sputtering

method and a step of performing thermal processing on said silicon layer to cause a metal layer composed of said metal material stacked on said silicon layer to react with said silicon layer.

C1 Cont.

13. (Withdrawn) The method for manufacturing the semiconductor device according to Claim 6, further comprising:

a step of stacking said silicon layer to be used for said pair of said electrode members on said semiconductor substrate;

a step of causing said silicon to become a silicide;

a step of implanting said impurity to be diffused into said silicide obtained through said step of causing said silicon to become a silicide;

a step of performing etching processing on said silicide to form said pair of said electrode members by using said silicide into which said impurity is implanted;

a step of stacking insulating materials to be used for said pair of said side walls on said pair of said electrode members and on portions exposed between said electrode members on said semiconductor substrate;

a step of implanting said impurity to be diffused into said insulating layer formed by stacking of said insulating materials;

a step of removing unwanted portions of said insulating layer with said impurity implanted to form said pair of said side walls facing each other at intervals;

a step of forming a gate electrode formed between said side walls on said semiconductor substrate with a gate insulator interposed between said gate electrode and said semiconductor substrate in a manner that both sides of said gate electrode are disposed on said both side walls; and

a step of thermally diffusing said impurity simultaneously from each of said pair of said electrode members with said

impurity implanted and from each of said pair of said side walls with said impurity implanted.

C1 Cont

15-23. (Cancelled)

24. (New) A MOS transistor, comprising:

a semiconductor substrate having a top surface;

isolation regions formed in said substrate;

a gate structure formed over said substrate having sidewalls disposed on either side of said gate structure;

a source region having a source lightly doped region and a source heavily doped drain region, wherein an impurity concentration of said source lightly doped region is lower than an impurity concentration of said source heavily doped region, wherein the source lightly doped region is formed below one of said sidewalls, wherein said heavily doped region is disposed between said source lightly doped region and said isolation region, and wherein a portion of said source lightly doped region extends beneath a gate oxide of said gate structure;

a drain region having a drain lightly doped region and a drain heavily doped region, wherein an impurity concentration of said drain lightly doped region is lower than an impurity concentration of said drain heavily doped region, wherein the drain lightly doped region is formed below one of said sidewalls, wherein said heavily doped drain region is disposed between said drain lightly doped region and said isolation region and wherein a portion of said drain lightly doped region extends beneath a gate oxide of said gate structure; and

metallic silicide layers respectively formed on said source heavily doped regions and said drain heavily doped regions, said metallic silicide layers being in contact with said sidewalls and said isolation regions, and extending onto said isolation regions, wherein undersides of said metallic silicide

layers are substantially coplanar with respective undersides of said sidewalls in contact with said top surface.

25. (New) A MOS transistor as recited in claim 24, wherein said metal silicide layers are formed between each of said sidewalls and said isolation regions.

C) Cont.

26. (New) The MOS transistor according to Claim 25, wherein said metal silicide layers have undergone implantation of an impurity by an ion implantation method prior to said thermal diffusion of said impurity and wherein said side walls are composed of insulating materials which has undergone implantation of an impurity by said ion implantation method prior to said thermal diffusion of said impurity from said side walls.

27. (New) The MOS transistor according to Claim 24, wherein an impurity concentration in said source lightly doped region is almost the same as that in said source heavily doped region.

28. (New) The MOS transistor according to Claim 24, wherein an impurity concentration in said source lightly doped region is substantially smaller than that in said source heavily doped region.

29. (New) The MOS transistor according to Claim 24, wherein an impurity concentration in said drain lightly doped region is almost the same as that in said drain heavily doped region.

30. (New) The MOS transistor according to Claim 24, wherein an impurity concentration in said drain lightly doped region is substantially smaller than that in said drain heavily doped region.

31. (New) The MOS transistor according to Claim 24, wherein each of said side walls extends, with its height being gradually decreased, on said semiconductor substrate in a direction in which both said side walls are brought near to each other from side portions of both said electrodes facing each other and wherein said gate electrode is formed in a manner that its both sides are disposed on said side walls.

C1 Cont.

32. (New) A semiconductor device, comprising:

a semiconductor substrate having a top surface;

isolation regions formed in said substrate, and which define active regions;

MOS transistors respectively disposed in said active regions, each of said MOS transistors having a gate structure, a source region, a drain region and sidewalls disposed on either side of each of said gate structures;

wherein each of said source regions has a source lightly doped region and a source heavily doped drain region, wherein an impurity concentration of said source lightly doped region is lower than an impurity concentration of said source heavily doped region, wherein the source lightly doped region is formed below one of said sidewalls, and wherein said heavily doped region is disposed between said source lightly doped region and one of said isolation regions;

wherein each of said drain regions has a drain lightly doped region and a drain heavily doped region, wherein an impurity concentration of said drain lightly doped region is lower than an impurity concentration of said drain heavily doped region, wherein the drain lightly doped region is formed below another of said sidewalls, and wherein said heavily doped drain region is disposed between said drain lightly doped region and said isolation region; and

metallic silicide layers respectively formed on said source heavily doped regions and said drain heavily doped regions, said metallic silicide layers being in contact with said sidewalls and said isolation regions, wherein undersides of said metallic silicide layers are substantially coplanar with respective undersides of said sidewalls in contact with said top surface.

C1 Cont

33. (New) A semiconductor device as recited in claim 32, wherein said metal silicide layers are formed between each of said sidewalls and said isolation regions.

34. (New) The semiconductor device according to Claim 32, wherein said metal silicide layers have undergone implantation of an impurity by an ion implantation method prior to said thermal diffusion of said impurity and wherein said side walls are composed of insulating materials which has undergone implantation of an impurity by said ion implantation method prior to said thermal diffusion of said impurity from said side walls.

35. (New) The semiconductor device according to Claim 32, wherein an impurity concentration in said source lightly doped regions is almost the same as that in said source heavily doped regions.

36. (New) The semiconductor device according to Claim 32, wherein an impurity concentration in said source lightly doped regions is substantially smaller than that in said source heavily doped regions.

37. (New) The semiconductor device according to Claim 32, wherein an impurity concentration in said drain lightly doped

regions is almost the same as that in said drain heavily doped regions.

38. (New) The semiconductor device according to Claim 32, wherein an impurity concentration in said drain lightly doped regions is substantially smaller than that in said drain heavily doped regions.

C1

39. (New) The semiconductor device according to Claim 32, wherein each of said side walls extends, with its height being gradually decreased, on said semiconductor substrate in a direction in which both said side walls are brought near to each other from side portions of both said electrodes facing each other and wherein said gate electrode is formed in a manner that its both sides are disposed on said side walls.